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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,323	01/05/2001	Masatoshi Akagawa	1081.1102	3680
21171	7590	04/11/2005	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			NGUYEN, KHIEM D	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/754,323	AKAGAWA, MASATOSHI	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 January 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 4-6, 14 and 16-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 14, 16 and 17 is/are allowed.
- 6) ☒ Claim(s) 4-6 and 18-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 January 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION*****Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 26<sup>th</sup>, 2005 has been entered. A new rejection is made as set forth in this Office Action. Claims (4-6, 14 and 16-21) are pending in the application.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

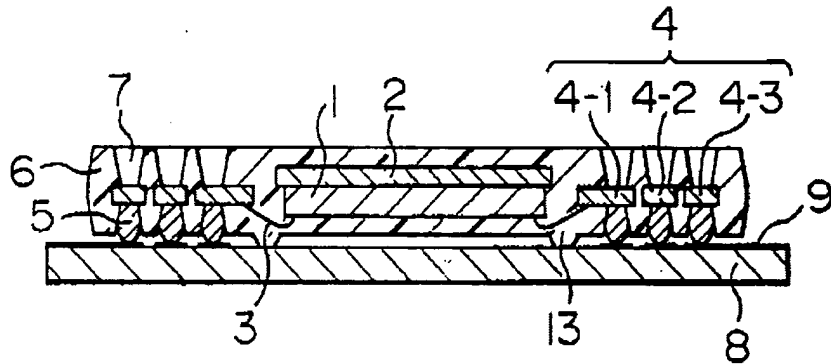
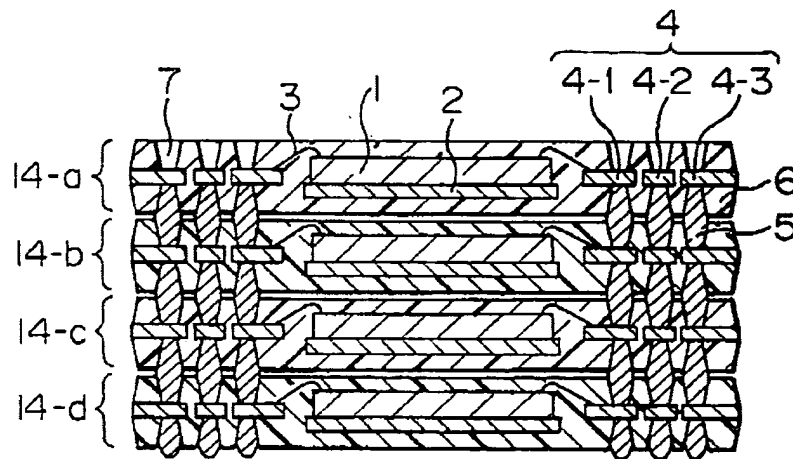
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitano et al. (U.S. Patent 5,608,265).

In re claim 18, **Kitano** discloses a semiconductor device comprising: a substrate having a main surface; a plurality of device layers (**14-a, 14-b, 14-c, 14d**) stacked in succession on the main surface of the substrate wherein each of the plural device layers comprises: a set of conductors comprising a wiring pattern (**3, 4-1, 4-2, 4-3**) (col. 5, line 63 to col. 6, line 10 and FIGS. 9-10); and insulating layer **6** formed on and embedding the

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set of conductors (3, 4-1, 4-2, 4-3) and having vias 7 extending therethrough (col. 6, lines 12-23 and FIGS. 9-10), and

**FIG. 9****FIG. 10**

wherein a wiring pattern of a first device layer is electrically connected to a first semiconductor element 1 embedded in a first insulating layer 6 with a first set of conductors (3, 4-1, 4-2, 4-3) and one or more of a second set of second set of conductors (located in the upper package 14-c, unlabeled) is/are electrically connected to the first semiconductor element 1 in a second insulating layer (located in the upper package 14-c,

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unlabeled) and through corresponding the vias 7 to one or more of the first set of conductors (col. 8, lines 10-27 and FIGS. 9-10).

In re claim 19, Kitano discloses that: the semiconductor elements 1 are commonly disposed within the respective insulating layers 6 and aligned in the plural, stacked device layers (packages 14-a, 14-b, 14-c, 14-d) (col. 5, line 63 to col. 6, line 23 and FIG. 10).

In re claim 20, Kitano discloses that the semiconductor device according to claim 18, further comprising: plural semiconductor elements 1 (one in each individual packages 14-a, 14-b, 14-c, 14-d) in each of the plural device layers and commonly disposed therein so as to be in aligned relationship in the stacked layers (col. 5, line 63 to col. 6, line 23 and FIG. 10).

In re claim 21, Kitano discloses that the semiconductor device according to claim 18, wherein each insulating layer 6 surrounds and covers “substantially” all of each outer surface of the semiconductor element 1 embedded therein (FIG. 10).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

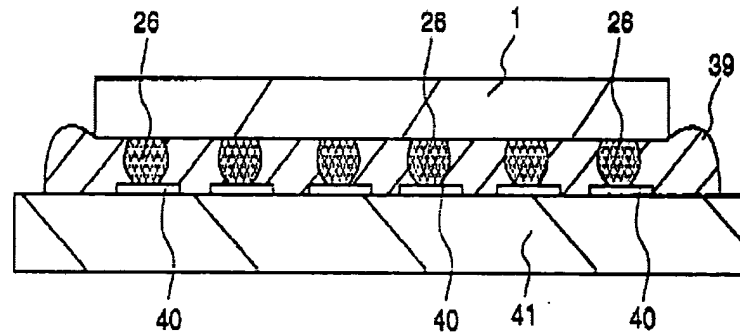
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitano et al. (U.S. Patent 5,608,265) in view of Itabashi et al. (U.S. Patent No. 6,300,244).

In re claim 4, it is held that the selection of the semiconductor element thickness is obvious because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species. In re Jones, 162USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA1980)(discovery of optimum value of result effective variable in a known process is obvious). Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

In re claims 5-6, Kitano does not explicitly disclose that each semiconductor element is electrically connected by flip chip mounting to respective wiring pattern and wherein each semiconductor element is electrically connected via an anisotropically conductive film to respective wiring pattern.

Itabashi discloses in figures 1-11 and related text that each semiconductor element 1 is electrically connected by flip chip mounting to respective wiring pattern, and inherently, by an anisotropically conductive film (figure 10 and col. 17, lines 10-30).

**FIG. 10**

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Itabashi with the method of Kitano in order to provide excellent anti-shock resistance and connection reliability (col. 3, lines 35-45, Itabashi).

***Allowable Subject Matter***

Claims 14, 16 and 17 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: (See Applicant's arguments in the Response submitted on July 27<sup>th</sup>, 2004, on page 2, lines 15-24).

***Response to Applicant's Amendment and Arguments***

Applicant contends that the amended independent claim 18 is not anticipated under 35 U.S.C. § 102(e) by Lauder et al. (U.S. Patent 6,130,823).

In response to Applicant's contention that the amended independent claim 18 is not anticipated under 35 U.S.C. § 102(e) by Lauder et al. (U.S. Patent 6,130,823), Examiner respectfully disagrees. Applicant's argument is moot since the newly

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discovered reference Kitano et al. (U.S. Patent 5,608,265) discloses the Applicant's claimed invention as recited in the independent claim 18 (Applicant is directed to page 2, 2<sup>nd</sup> paragraph to page 3, 2<sup>nd</sup> paragraph presented in this Office Action).

For this reason, examiner holds the rejection proper.

*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.  
April 06<sup>th</sup>, 2005



W. DAVID COLEMAN  
PRIMARY EXAMINER